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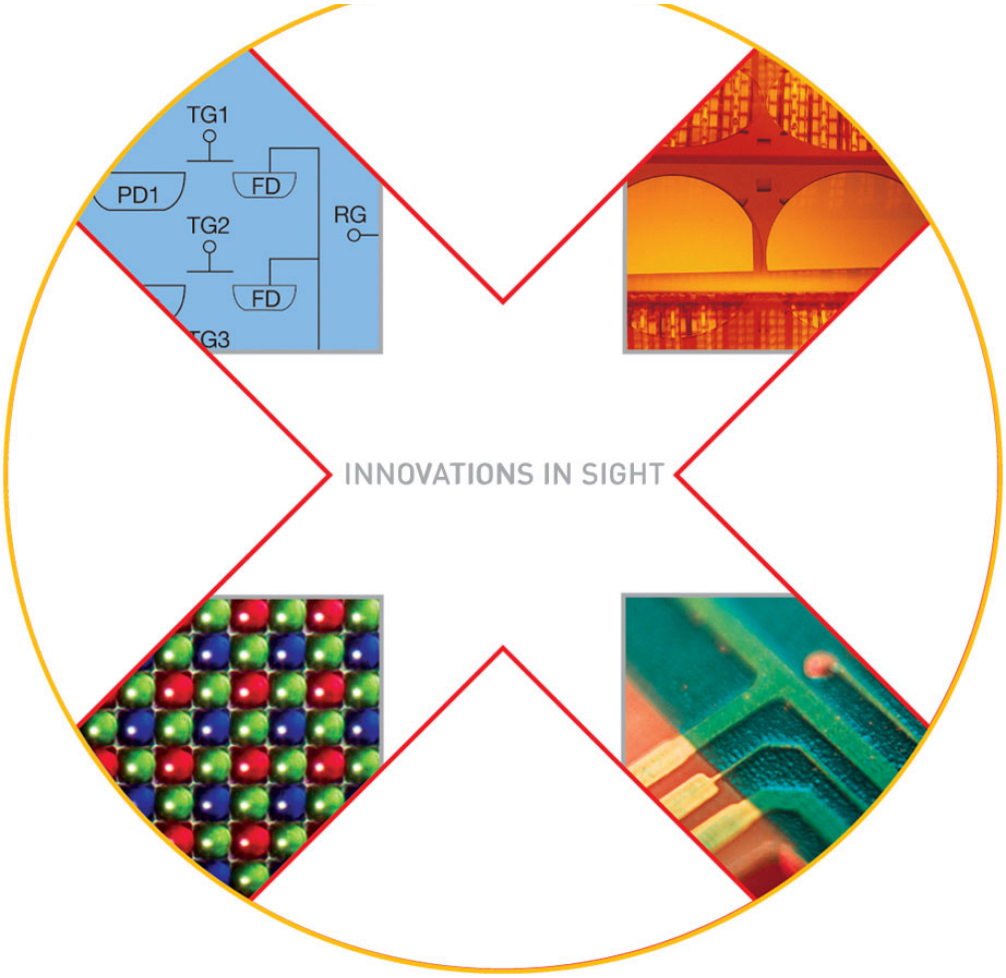
Image Sensor Solutions

PRELIMINARY DEVICE PERFORMANCE SPECIFICATION

Revision 0.2

March 2, 2006

PRELIMINARY



KODAK KAF-09000 IMAGE SENSOR

3056 (H) X 3056 (V) FULL-FRAME CCD IMAGE SENSOR

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TABLE OF CONTENTS

PRELIMINARY

TABLE OF FIGURES

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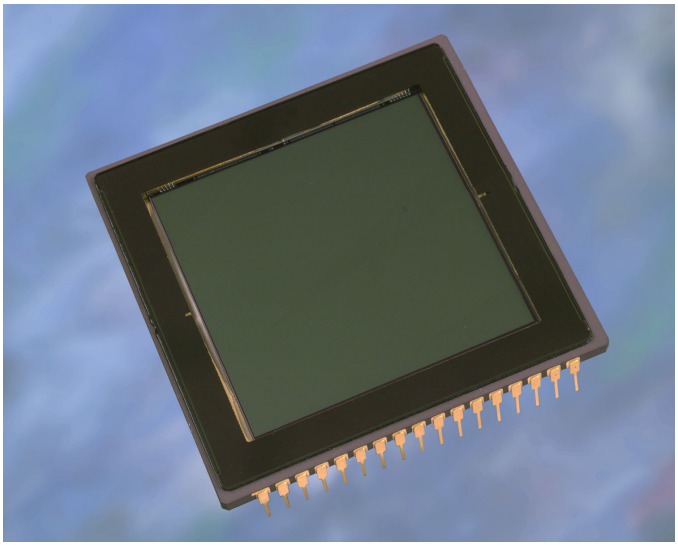
SUMMARY SPECIFICATION PRELIMINARY

KODAK KAF-09000 IMAGE SENSOR

3056 (H) X 3056 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

The KAF-09000 is a high performance monochrome area CCD (charge-coupled device) image sensor with 3056H x 3056V photo active pixels designed for a wide range of image sensing applications in the 0.4 nm to 1.0 nm wavelength band. Typical applications include scientific, and industrial imaging. Each pixel contains anti-blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Total chip size is 38.60 mm x 37.76 mm and is housed in a 34-pin, 2.010" wide DIL ceramic package with 0.1" pin spacing.



Features

- High resolution
- Broad dynamic range
- Low noise
- Large active imaging area

APPLICATIONS

- Digital radiography

Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	3103 (H) x 3086 (V)
Number of Effective Pixels	3085 (H) x 3085 (V) = 9.5 M
Number of Active Pixels	3056(H) x 3056 (V) = 9 M
Pixel Size	12 µm (H) x 12 µm (V)
Chip Size	38.6 mm (H) x 37.76mm (V)
Aspect Ratio	square
Saturation Signal	120 K e^-
Charge to Voltage Conversion	24 µV/e^-
Quantum Efficiency (550nm))	64%
Read Noise (f=4 MHz)	7 e^-
Dark Signal (T=25°C)	10 e/pix/sec
Dark Current Doubling Temperature	7° C
Linear Dynamic Range (f=4 MHz)	84 dB
Blooming Protection (4ms exposure time)	> 100X saturation exposure
Maximum Data Rate	10 MHz

Values in green have changed from past versions of this document.

PRELIMINARY

DEVICE DESCRIPTION

ARCHITECTURE

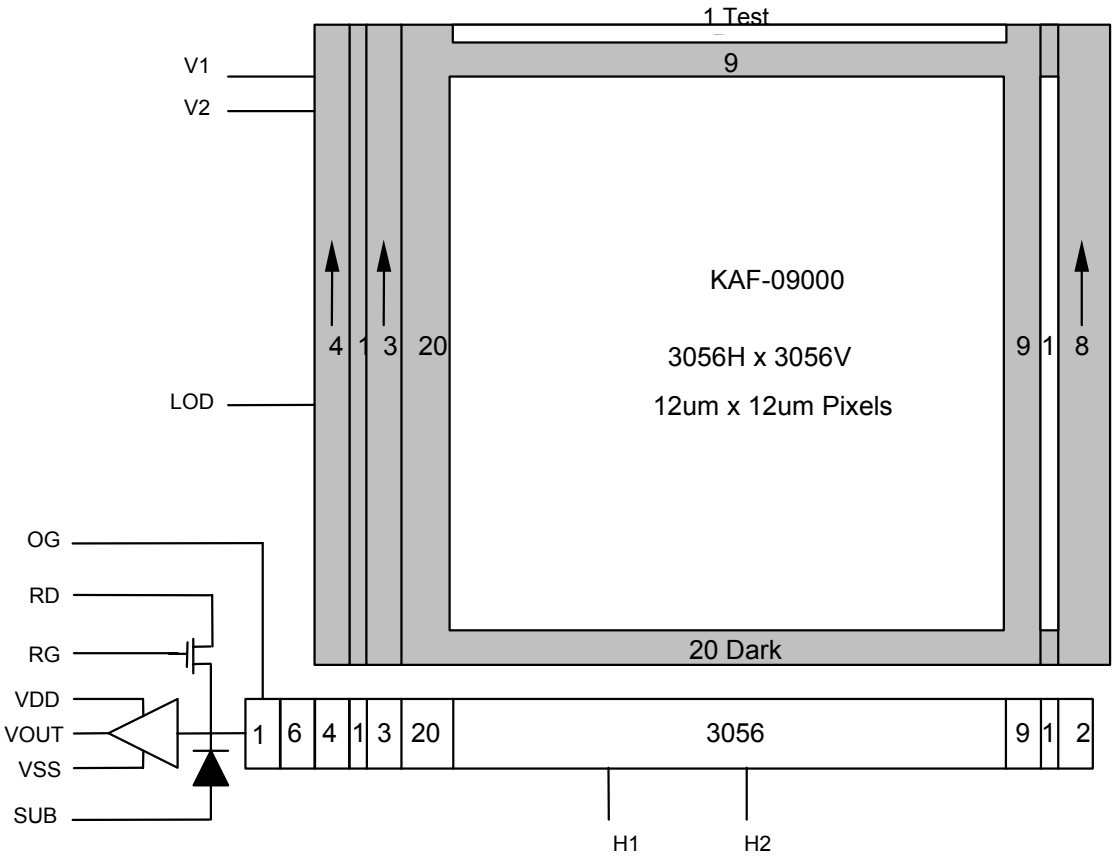


Figure 1 - Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 20 leading dark pixels on every line. There are also 20 full dark lines at the start and 9 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

Dummy Pixels

Within each horizontal shift register there are 11 leading pixels. These are designated as *dummy pixels* and should not be used to determine a dark reference level.

Internal Test

There are some pixels within each line that may not represent dark signal or the signal in the dummy pixels. These are introduced into the design to facilitate production testing. These behave differently than the

buffer and dark pixels and should not be used to establish a dark reference.

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each pixel is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion.

PRELIMINARY

HORIZONTAL REGISTER

Output Structure

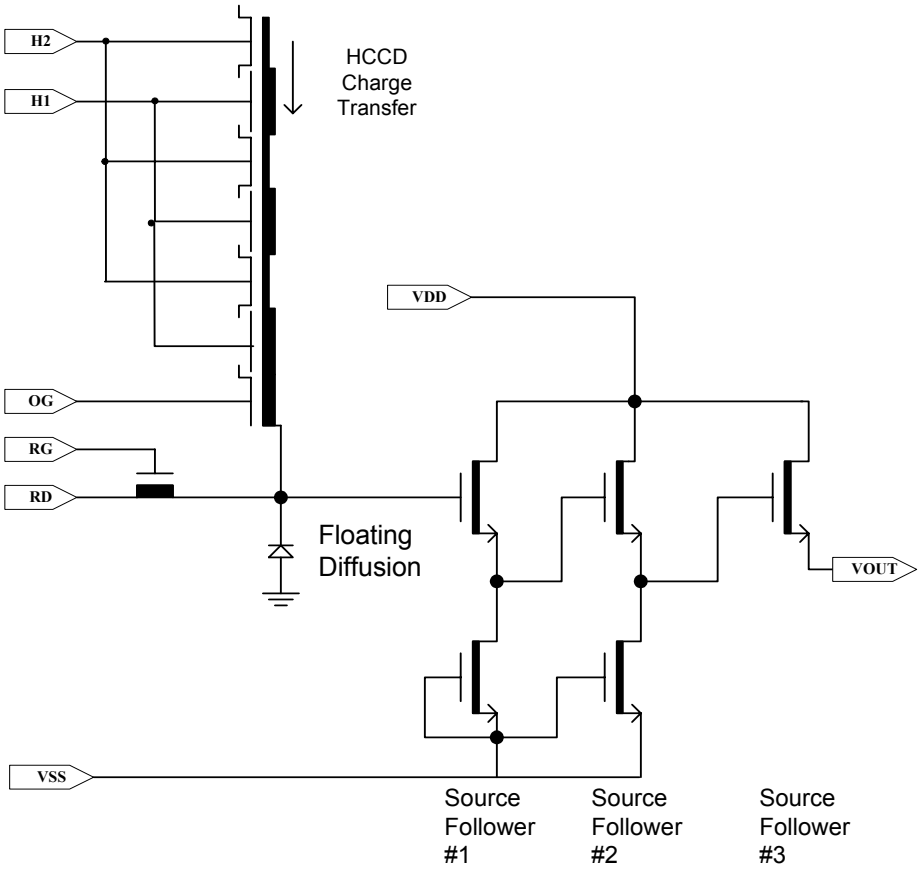


Figure 2 - Output Architecture

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 3.

PRELIMINARY

Output Load

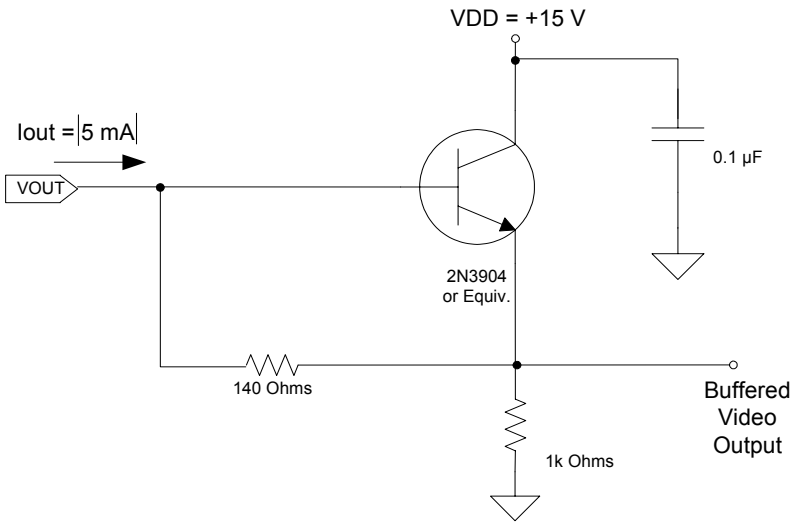
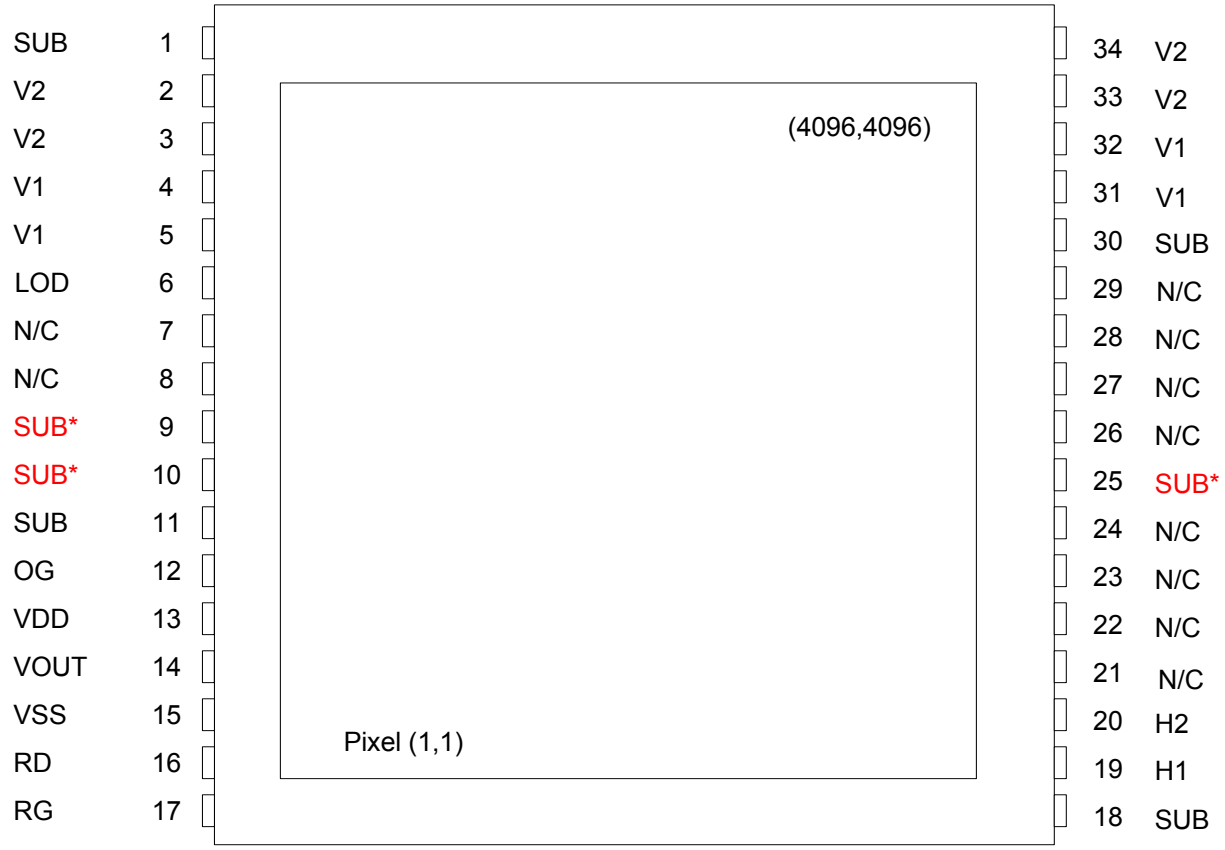


Figure 3 - Recommended Output Structure Load Diagram.
Note: Component values may be revised based on operating conditions and other design considerations.

PRELIMINARY

PHYSICAL DESCRIPTION

Pin Description and Device Orientation



Note: Pins with the same name are to be tied together on the circuit board and have the same timing.

PRELIMINARY

Pin	Name	Description
1	SUB	Substrate
2	V2	Vertical CCD Clock-Phase 2
3	V2	Vertical CCD Clock-Phase 2
4	V1	Vertical CCD Clock-Phase 1
5	V1	Vertical CCD Clock-Phase 1
6	LOD	Anti Blooming Drain
7	N/C	No Connection
8	N/C	No Connection
9	SUB* [1]	No Connection
10	SUB* [1]	No Connection
11	SUB	Substrate
12	OG	Output Gate
13	VDD	Output Amplifier Supply
14	VOUT	Video Output:
15	VSS	Output Amplifier Return
16	RD	Reset Drain
17	RG	Reset Gate
18	SUB	Substrate
19	H1	Horizontal Phase 1
20	H2	Horizontal Phase 2
21	N/C	No Connection
22	N/C	No Connection
23	N/C	No Connection
24	N/C	No Connection
25	SUB* [1]	No Connection
26	N/C	No Connection
27	N/C	No Connection
28	N/C	No Connection
29	N/C	No Connection
30	SUB	Substrate
31	V1	Vertical CCD Clock-Phase 1
32	V1	Vertical CCD Clock-Phase 1
33	V2	Vertical CCD Clock-Phase 2
34	V2	Vertical CCD Clock-Phase 2

Notes:

Pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating

PRELIMINARY

PERFORMANCE

IMAGE PERFORMANCE OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Frame time ($t_{readout}$ + t_{int})		Includes overclock pixels
Integration time (tint)	variable	
Horizontal clock frequency	4 MHz	
Temperature	> 20°C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width t_{VW} = 20 µs	

IMAGE PERFORMANCE SPECIFICATIONS

The parameters in green and violet reflect measured values. The green values have changed from the design predictions, the violet values have not changed and are as predicted. Other values are predicted (not yet measured) values.

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan
Saturation Signal	Ne^-_{sat}		120k		e^-		die
Quantum Efficiency 550 nm	Rg		64		%QE	1	design
Photoresponse Non-Linearity	PRNL		1		%	2	
Photoresponse Non-Uniformity	PRNU		1		%	3	
Integration Dark Signal	Vdark,int		5 0.7	17 2	e/pix/sec pA/cm^2	4	die
Read out Dark Signal	Vdark,read		80		electrons	5	die
Dark Signal Non-Uniformity	DSNU			50	e/pix/sec	6	die
Dark Signal Doubling Temperature	ΔT		7		°C		design
Read Noise	NR		7		e^- rms	7	die
Linear Dynamic Range	DR		84		dB	8	design
Blooming Protection	X_ab	100			x Esat	9	design
Output Amplifier Sensitivity	Vout/Ne^-		24		µV/e		
DC Offset, output amplifier	Vodc		Vrd-0.5		V	10	die
Output Amplifier Bandwidth	f_{-3dB}		88		MHz		design
Output Impedance, Amplifier	ROUT		180		Ohms		die

Notes:

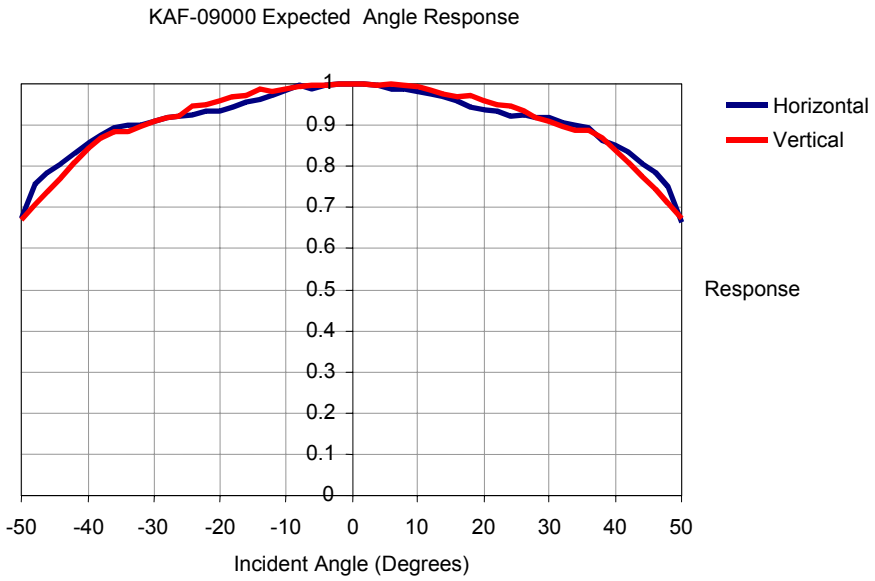
1. Increasing output load currents to improve bandwidth will decrease these values.

2. Worst case deviation from straight line fit, between 1% and 90% of Vsatmin.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 °C.
5. Read out dark current depends on the read out time, primarily when the vertical CCD clocks are at their high levels. This is approximately 0.125 sec/image for nominal timing conditions. The readout dark current is also dependent on the operating temperature. The specification applies to 25 °C.
6. Average dark signal of any of 32 x 32 blocks within the sensor. (each block is 128 x 128 pixels)
7. Output amplifier noise only. Operating at pixel frequency up to 4MHz, bandwidth <20MHz , tint = 0, and no dark current shot noise.
8. $20\log(Vsat/V_N)$
9. X_ab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_ab is measured at 4ms.
10. Video level offset with respect to ground.

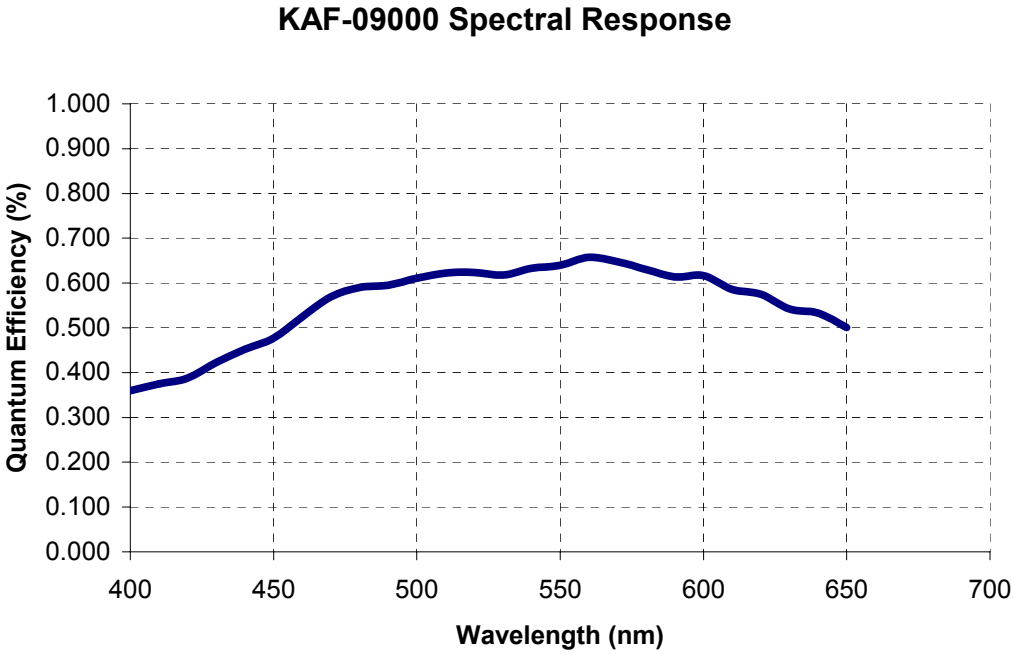
PRELIMINARY

TYPICAL PERFORMANCE

ANGLE RESPONSE - ESTIMATED

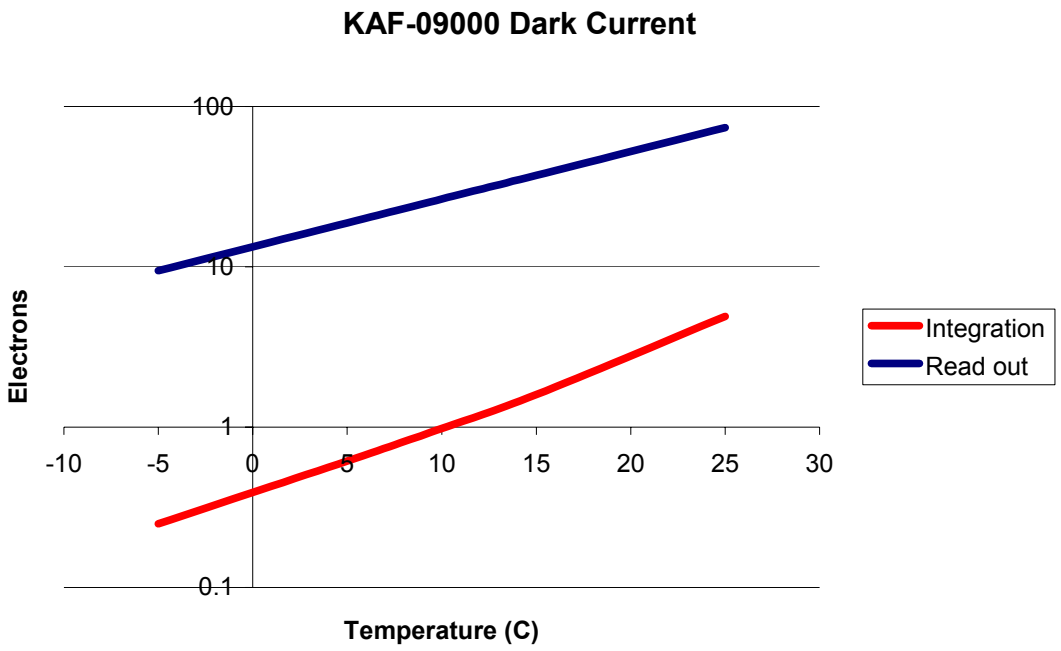


SPECTRAL RESPONSE - MEASURED

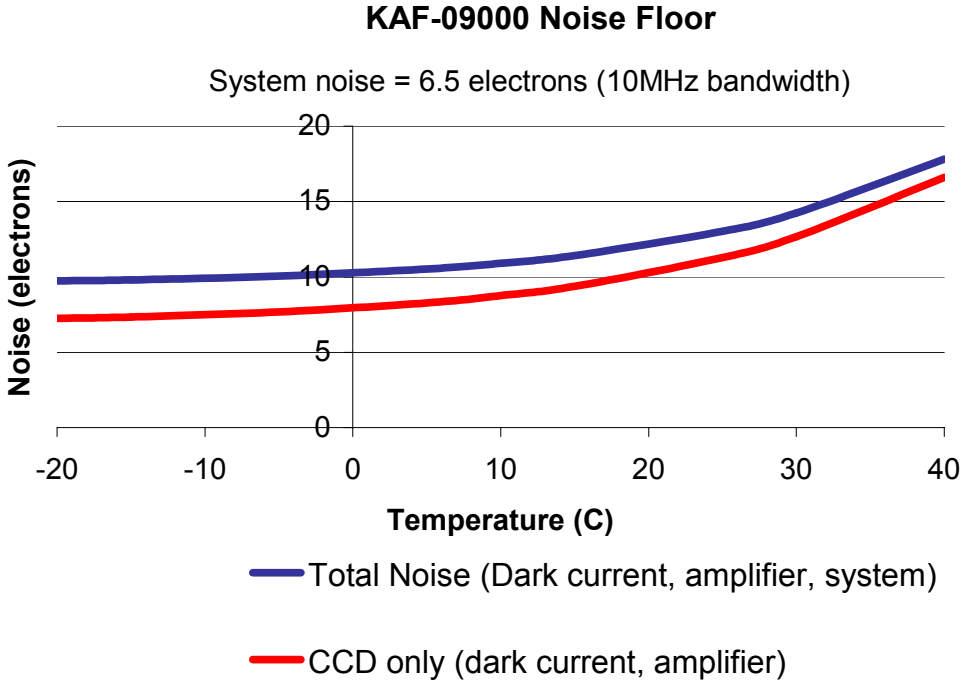


PRELIMINARY

DARK SIGNAL - MEASURED

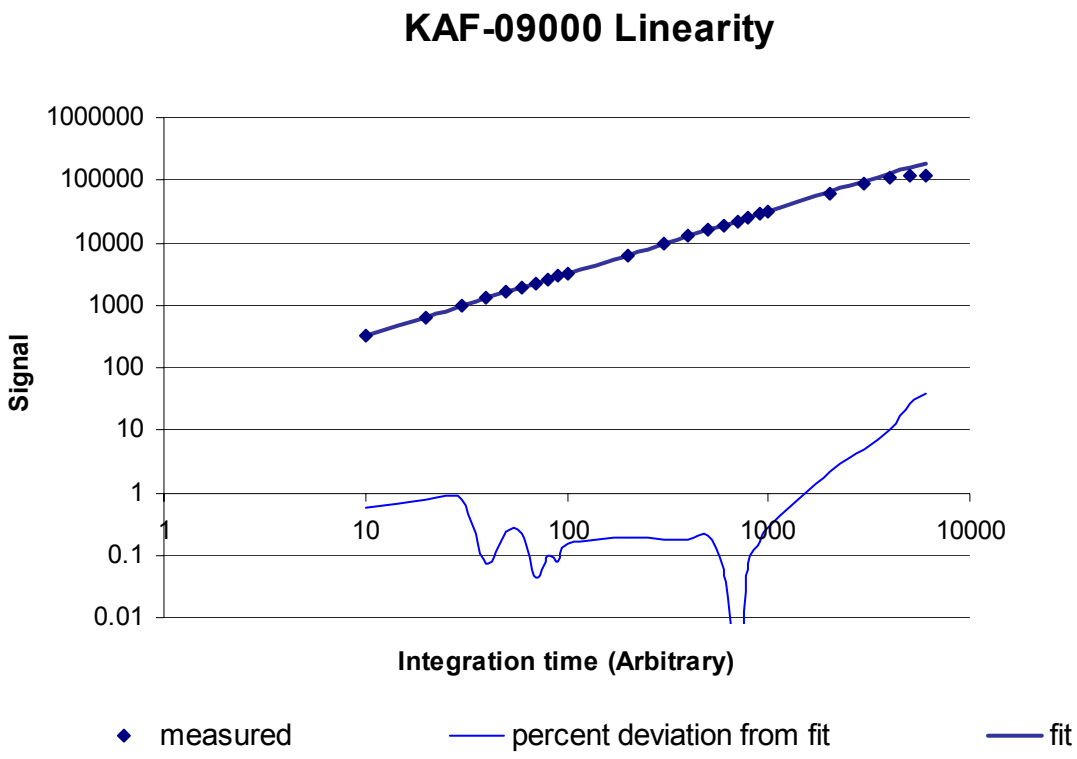


NOISE FLOOR - MEASURED



PRELIMINARY

LINEARITY - MEASURED



PRELIMINARY

COSMETIC PERFORMANCE

Cosmetic Operational Conditions

All cosmetic tests performed at T ~25 °C

Cosmetic Specifications

Points	Clusters	Columns
<200	<20	<10

Cosmetic Definitions

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

-- OR --

Bright: A Pixel with dark current > 7,000 e/pixel/sec at 25C

Cluster Defect

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of more than 10 point defects along a single column

-- OR --

A column containing a pixel with dark current > 20,000e/pixel/sec (bright column)

-- OR --

A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 Ke

A pixel which loses more than 250 e under 2Ke illumination (trap defect)

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

PRELIMINARY

OPERATION

ABSOLUTE MAXIMUM RATINGS[8]

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+20	V	1,2
Adjacent Gate Pin Voltages	V_{gate1}	-13.5	+13.5	V	1,3
Isolated Gate Pin Voltages	V_{1-2}	-0.5	+13.5	V	4
Output Bias Current	I_{out}		-30	mA	5
LOD Diode Voltage	V_{LODT}	-0.5	+13.0	V	6
Operating Temperature	T_{OP}	-60	60	°C	7

Notes:

1. Referenced to pin VSUB
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H2, VOG.
4. Includes pins: RG.
5. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
6. V1, H1, V2, H2, H1L, VOG, and VRD are tied to 0 V.
7. Noise performance will degrade at higher temperatures due to dark current increasing .
8. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

PRELIMINARY

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}		13		V	I_{RD} = 0.01	
Output Amplifier Return	VV_{SS}		2.0		V	I_{SS} = 3.0	
Output Amplifier Supply	VV_{DD}		15.0		V	I_{OUT} + I_{SS}	
Substrate	V_{SUB}		0		V	0.01	
Output Gate	V_{OG}	0	1	2	V	0.01	
Lateral Overflow Drain	V_{LOD}		10.0		V	0.01	
Video Output Current	I_{OUT}		-5		mA		1

Notes:

1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 3.

AC OPERATING CONDITIONS –

Values in green have changed from previous versions of this document.

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low		-9.0		V	250 nF	1
V1 High Level	V1H	High		2.5		V		1
V2 Low Level	V2L	Low		-9.0		V	250 nF	1
V2 High Level	V2H	High		2.5		V		1
H1 Low Level	H1L	Low		-2		V	500 pF	1
H1 High Level	H1H	High		8		V		1
H2 Low Level	H2L	Low		-2		V	300 pF	1
H2 High Level	H2H	High		8		V		1
RG Low Level	V_{RGL}	Low		6		V	13 pF	1
RG High Level	V_{RGH}	High		11		V		1

Notes:

1. All pins draw less than 10 µA DC current. Capacitance values relative to SUB (substrate).

PRELIMINARY

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H		4	10	MHz	1
H1, H2 Rise, Fall Times	t_{H1r} , t_{H1f}	5			%	3
V1, V2 Rise, Fall Times	t_{V1r} , t_{V1f}	5			%	3
V1 - V2 Cross-over	V_{VCR}	-1	0	1	V	
H1 - H2 Cross-over	V_{HCR}			0	V	
H1, H2 Setup Time	t_{HS}	1	5		µs	
RG Clock Pulse Width	t_{RGw}	5			ns	4
V1, V2 Clock Pulse Width	t_{Vw}		20		µs	

Timing Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Pixel Period (1 Count)	t_e		250		ns	2
Integration Time	t_{int}		-			5
Line Time	t_{line}		0.821		ms	6
Readout Time	$t_{readout}$		2,533		ms	7

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. $(3103 * t_e) + t_{HS} + (2 * t_{Vw}) = 0.821$ msec
7. $t_{readout} = t_{line} * 3086$ lines.
8. Measured where Vclock is at 0 volts

PRELIMINARY

Frame Timing

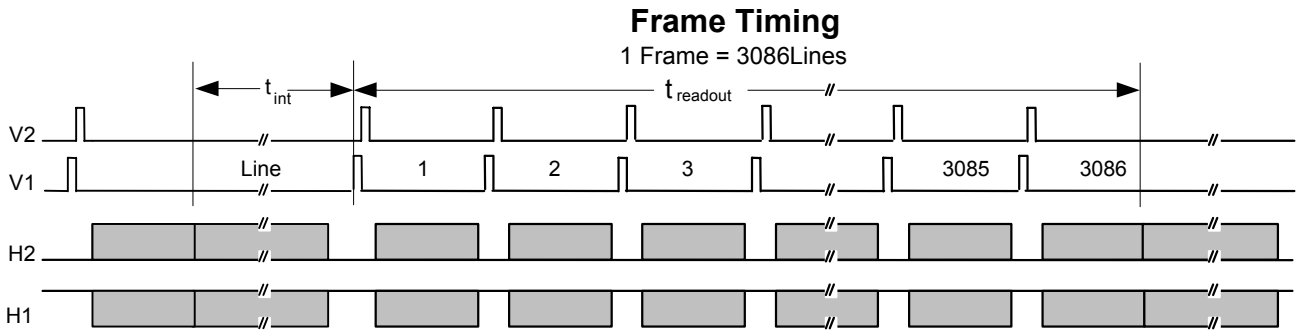


Figure 4 - Frame Timing

Frame Timing Detail

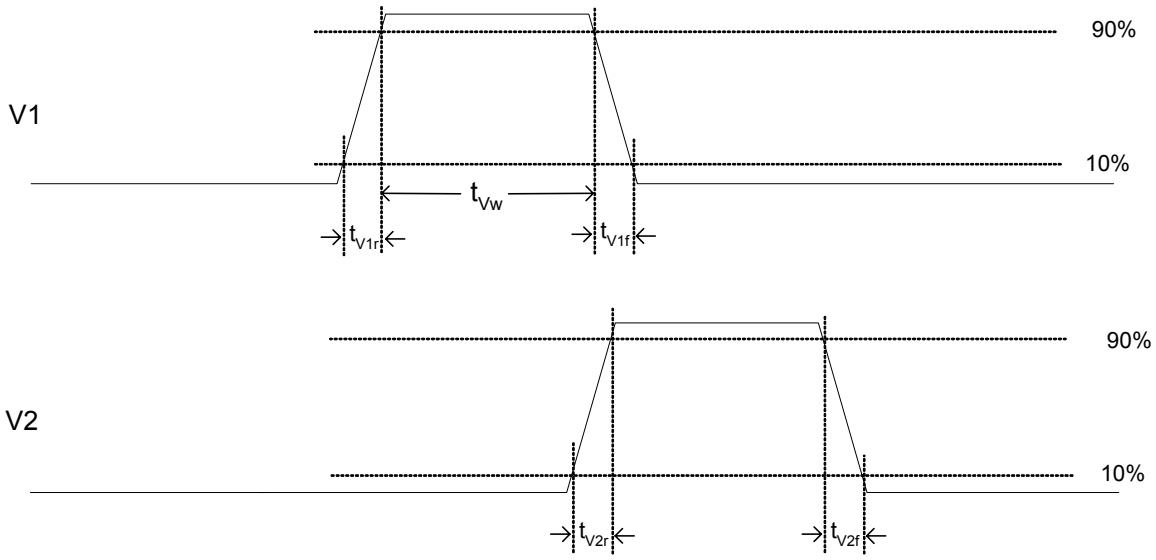


Figure 5 - Frame Timing Detail

PRELIMINARY

Line Timing

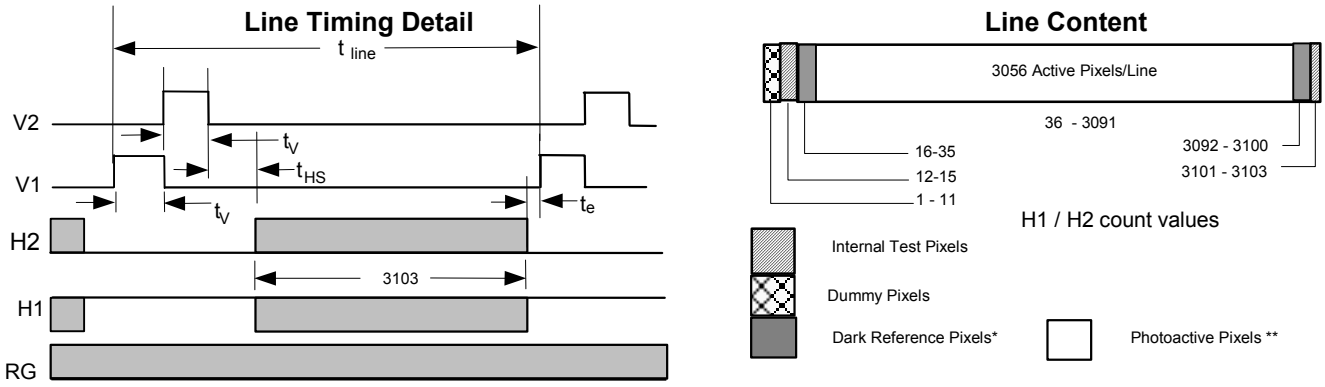


Figure 6 - Line Timing

Pixel Timing Detail

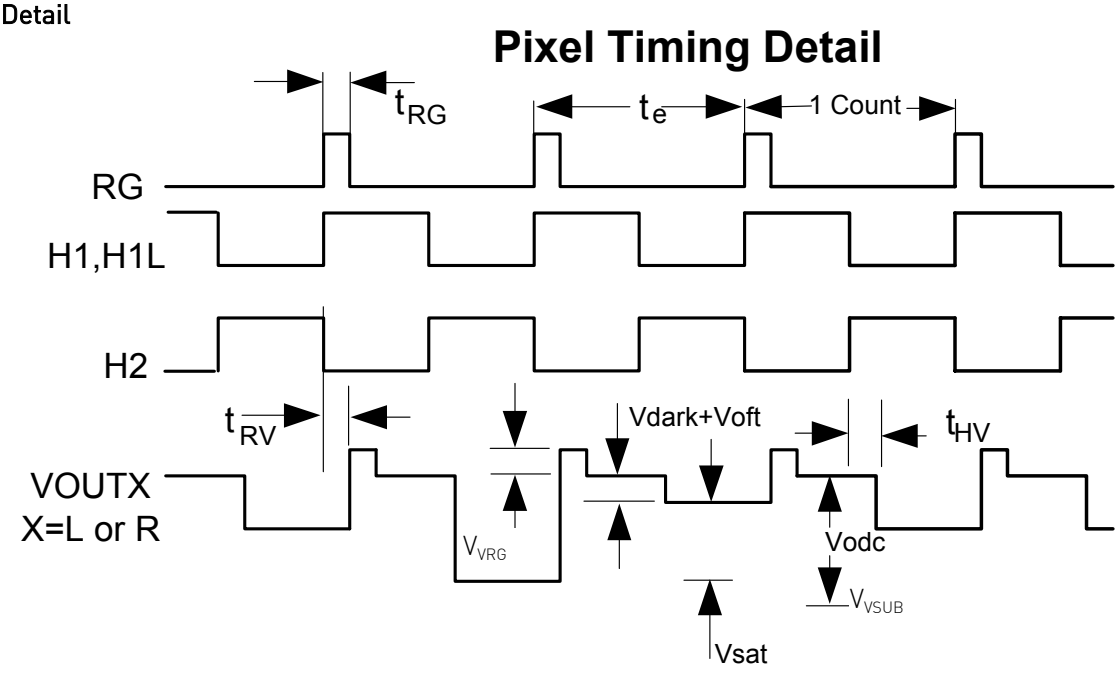


Figure 7 – Pixel Timing

PRELIMINARY

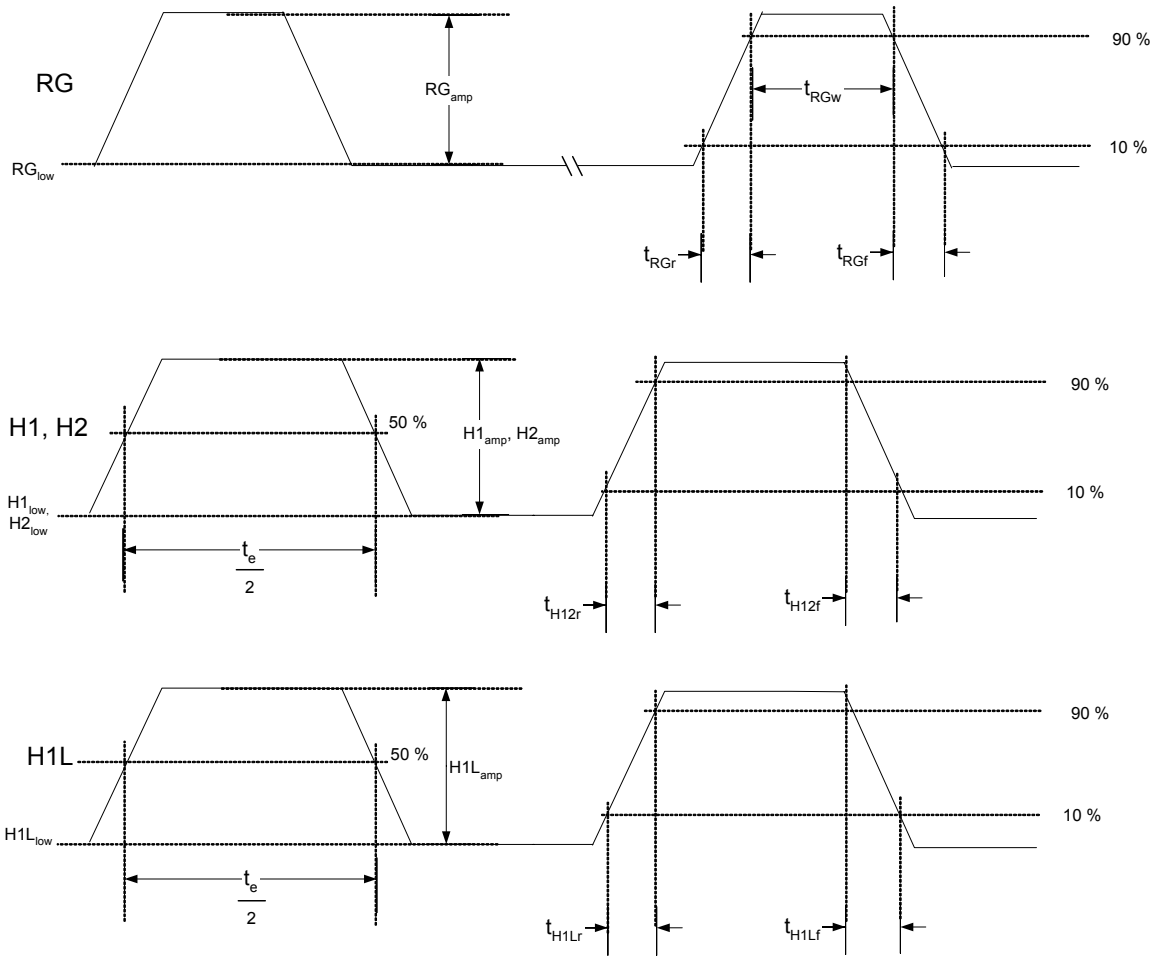


Figure 8 - Pixel Timing Detail

PRELIMINARY

Timing Edge Alignment

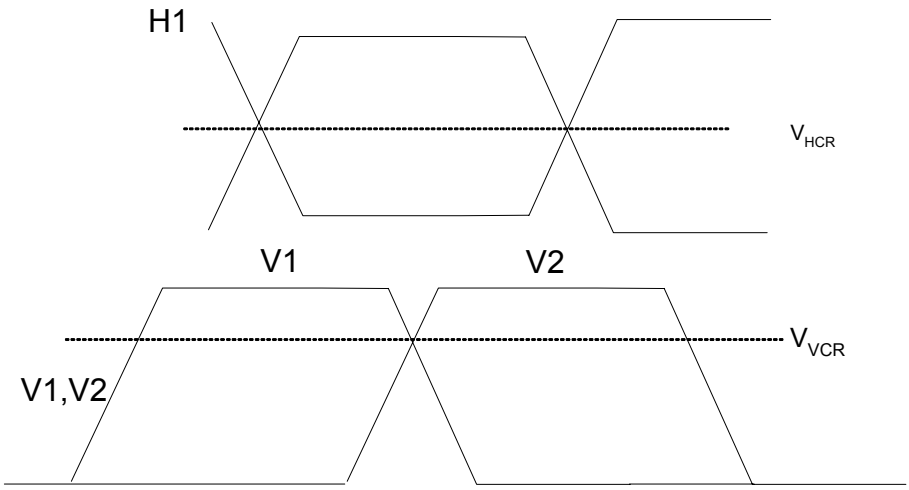


Figure 9 - Timing Edge Alignment

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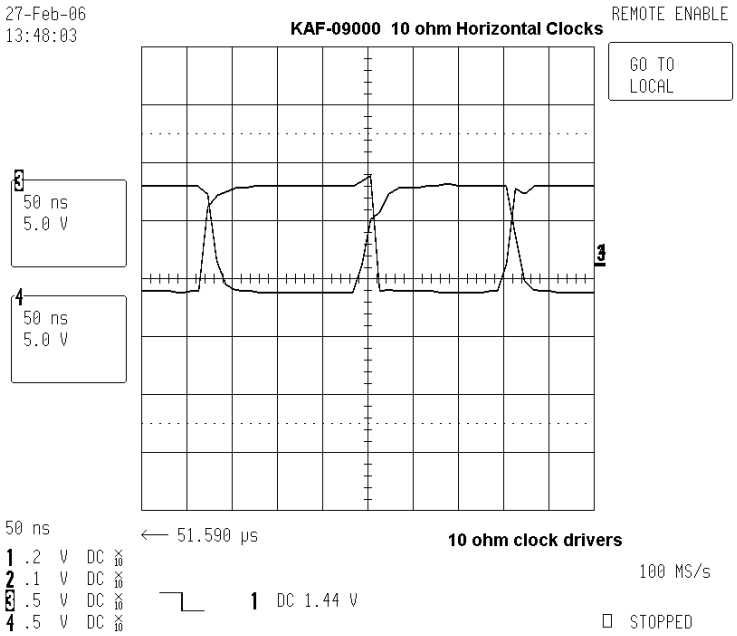
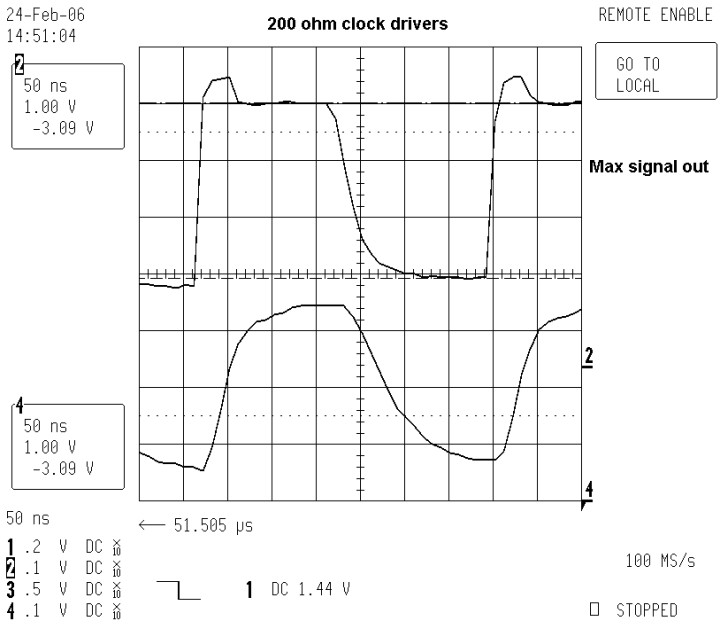
PRELIMINARY

EXAMPLE WAVEFORMS

Horizontal CCD clocks

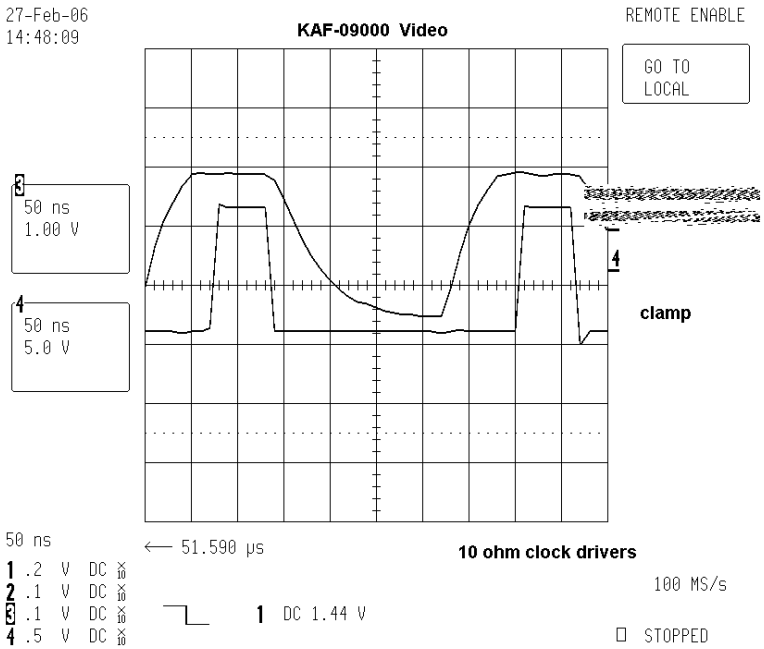


Video Waveform – at the CCD output and bandwidth limited at the analog to digital converter.

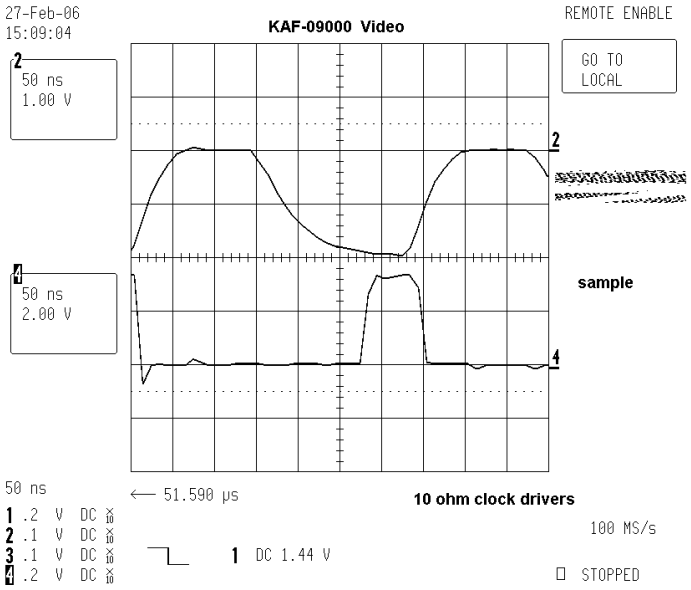


PRELIMINARY

Video waveform and clamp clock



Video waveform and sample clock



PRELIMINARY

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	°C	1

Note:

1. Long-term storage toward the maximum temperature will accelerate color filter degradation

ESD

This device contains limited protection against Electrostatic Discharge (ESD) and is rated as a Class 0 device, JESD22 Human Body, and Class A, JESD22 Machine Mode

Devices should be handled in accordance with strict handling precautions. See ISS Application Note MTD/PS-0224, "Electrostatic Discharge Control".

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.

Caution: Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237, "Cover Glass Cleaning Procedure for Image Sensors"

SOLDERING RECOMMENDATIONS

Partial Heating Method: 280 °C maximum pin temperature; 10 seconds maximum duration per pin.

PRELIMINARY

MECHANICAL DRAWINGS

PACKAGE

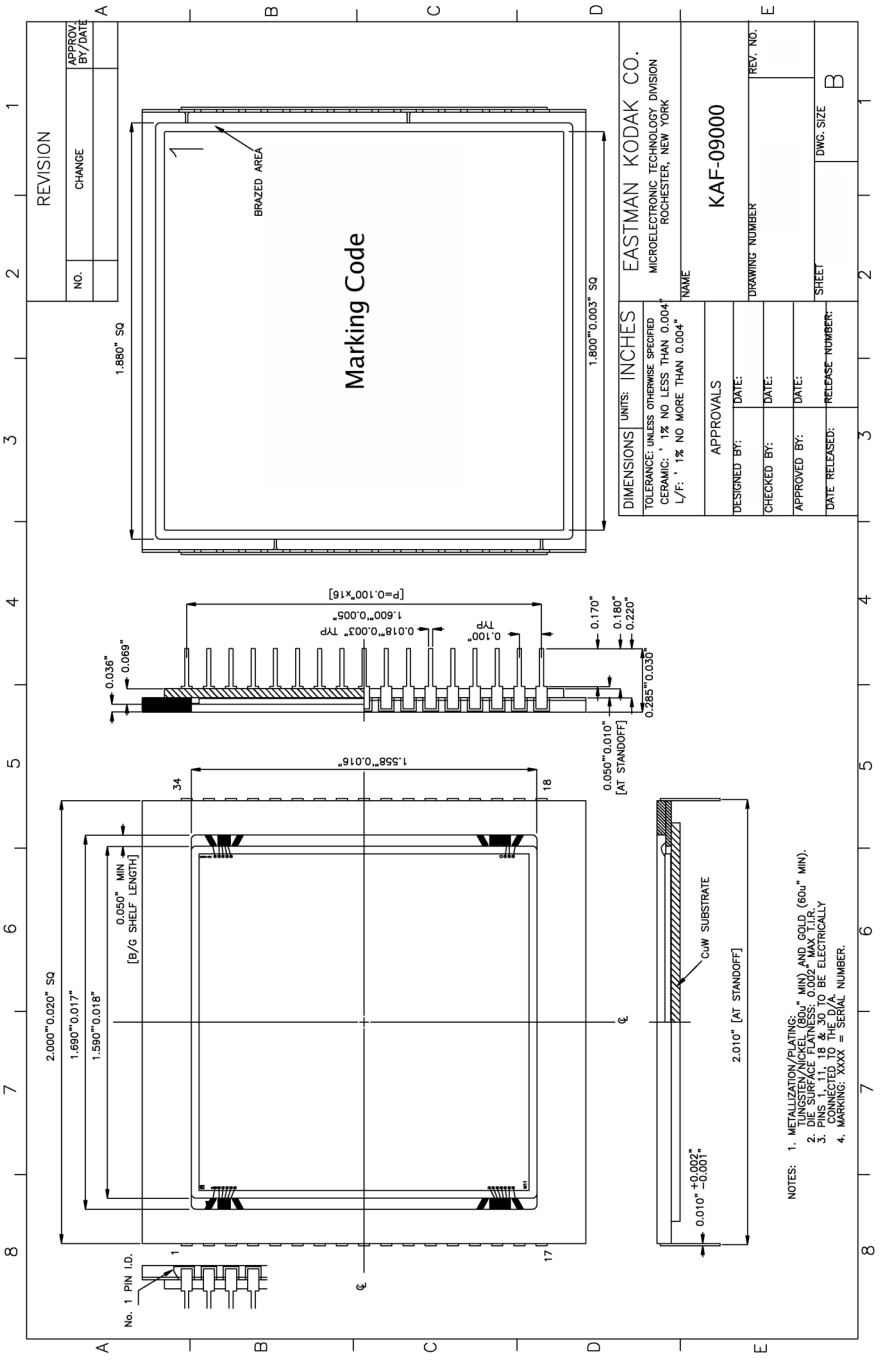


Figure 10 – Completed Assembly Drawing

PRELIMINARY

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

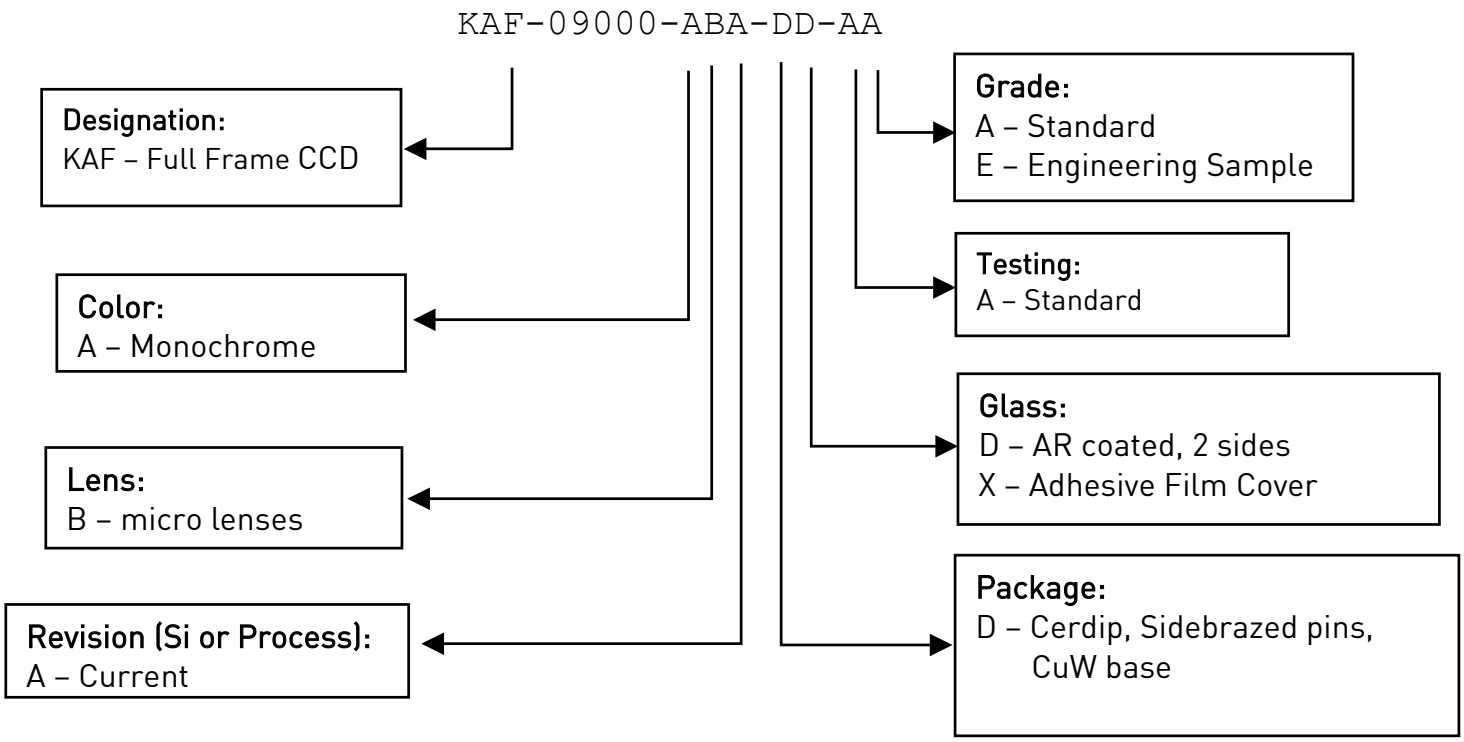
Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

PRELIMINARY

AVAILABLE PART CONFIGURATIONS

Available Part Numbers
KAF-09000-ABA-DD-AA
KAF-09000-ABA-DD-AE
KAF-09000-ABA-DX-AA
KAF-09000-ABA-DX-AE



Please contact Image Sensor Solutions for available part numbers.

PRELIMINARY

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
0.1	First Preliminary version
0.2	Fixed available part number formatting and glass designator, added internal SUB pin labels Updated measured parameters Updated operating voltages Added Spectral response, noise, dark current, and linearity plots

PRELIMINARY

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